CRADA 0606 – Final Report

Direct To Digital Holography

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Abstract

In this CRADA, Oak Ridge National Laboratory (ORNL) assisted nLine Corporation of Austin, TX in the development of prototype semiconductor wafer inspection tools based on the direct-to-digital holographic (DDH) techniques invented at ORNL. Key components of this work included, development of the first prototype named the Visible Alpha Tool (VAT) that uses visible spectrum illumination of 532nm, assist in design of second prototype tool named the DUV Alpha Tool (DAT) using deep UV (266nm) illumination, and continuing support of nLine in the development of higher throughput commercial tools.

Statement of Objectives

At the start of this CRADA, nLine Corporation was a new company started with venture capital funding based on the DDH techniques. nLine had plans to develop four prototype tools based on direct-to-digital holographic (DDH) techniques invented at Oak Ridge National Laboratory (ORNL).

The first objective of this project was to develop, design, and fabricate a working engineering proof of principle DDH inspection tool. This first prototype used a laser in the visible spectra (532 nm) and is called the Visible Alpha Tool (VAT). The primary goals of the VAT development were to show that the DDH system works with improved optics (noise is significantly reduced) and that, through die-to-die comparisons, defects on the order of ~150nm (depending on laser selected) can be detected in a reasonable time (about 1/2 day.) Some features of the VAT are a visible laser (532 nm), 1 Mpixel CCD camera, autofocus, manual wafer handling, automated wafer registration and image capture, and a low throughput rate.

The second objective of this CRADA was to assist nLine in development of the computing system architecture for the Early Adopter Tool (EAT) and the DUV BETA Tool (BETA I). These two tools are the first commercial versions of the inspection system and operate at speeds of 15 and 30 frames per second.

The third and final objective was to assist with any image processing issues that might arise in the reconstruction and defect detection algorithms particular to the various wafer types to be inspected.

Benefits to DOE Office's Mission

The project addresses DOE mission in two major ways. First, the development of new inspection tools for the semiconductor manufacturing environment has the potential for reductions in energy consumption during manufacturing. Second, this project supports the development of new technical business in the United States and moves technology developed at a DOE lab into the commercial sector.

Technical Discussion of Work Performed

As mentioned in the objective section, this project was broken into three major areas: VAT development, processing design for next generation tool, and support of image reconstruction and defect detection algorithm development.

VAT Development
The overall VAT project was broken into three technical tasks. The tasks and their ORNL leaders are shown in Figure 1.

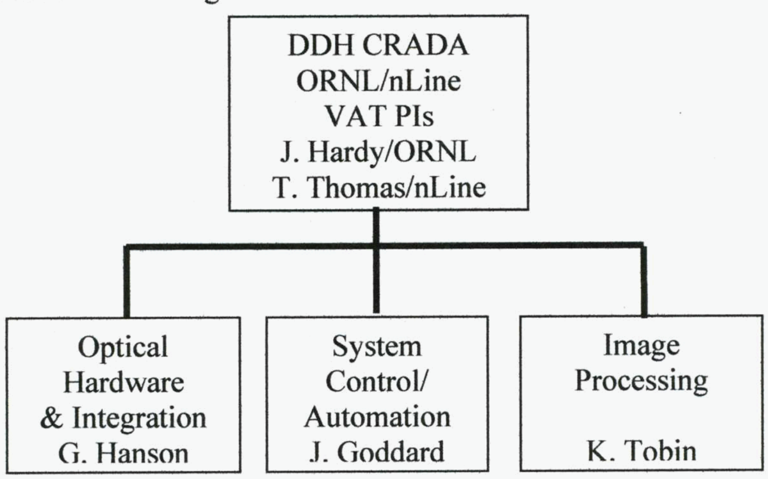

Figure 1. Overall Work Breakdown Structure for the VAT project

In conjunction with an nLine employee (T. Thomas) ORNL co-designed the optical system for the VAT, wrote specifications for the hardware, designed and developed the control system hardware and software, and designed and developed the image processing algorithms and software. At the completion of this task the VAT was operational for die to die defect detection on 200mm semiconductor wafers. Figure 2 shows a picture of the VAT stage and optical system. While the VAT requires manual loading and unloading of wafers, it is capable of long inspection cycles (>8 hours) enabling full inspection of wafers.

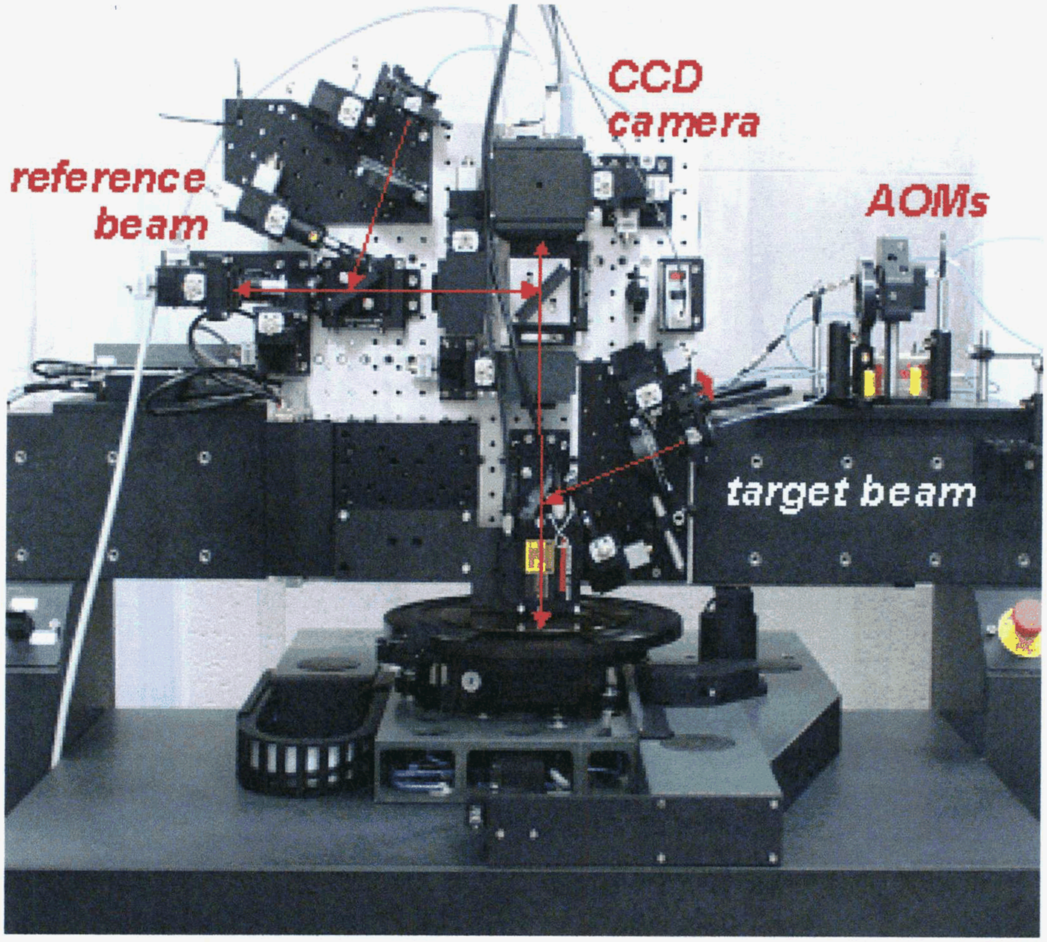

Figure 2. VAT stage and optical system

VAT Hardware Development

The hardware development subtask spanned a wide range of responsibilities. First, a lab was prepared for the tool development with the acquisition and installation of a softwall cleanroom that remains as an excellent lab environment for use on other projects. Second, ORNL worked with nLine to obtain custom optics for the VAT in an attempt to further reduce noise and improve resolution of the system. This involved specifying the desired qualities of the optical system, working with optical designers to get final designs, acquiring components for the optical train, and testing the optical subsystem. Figure 3 shows the basic optical layout generated in this task. Third, the mechanical motion systems needed for scanning the wafer, movement of optics were specified, acquired, tested, and assembled under this subtask.

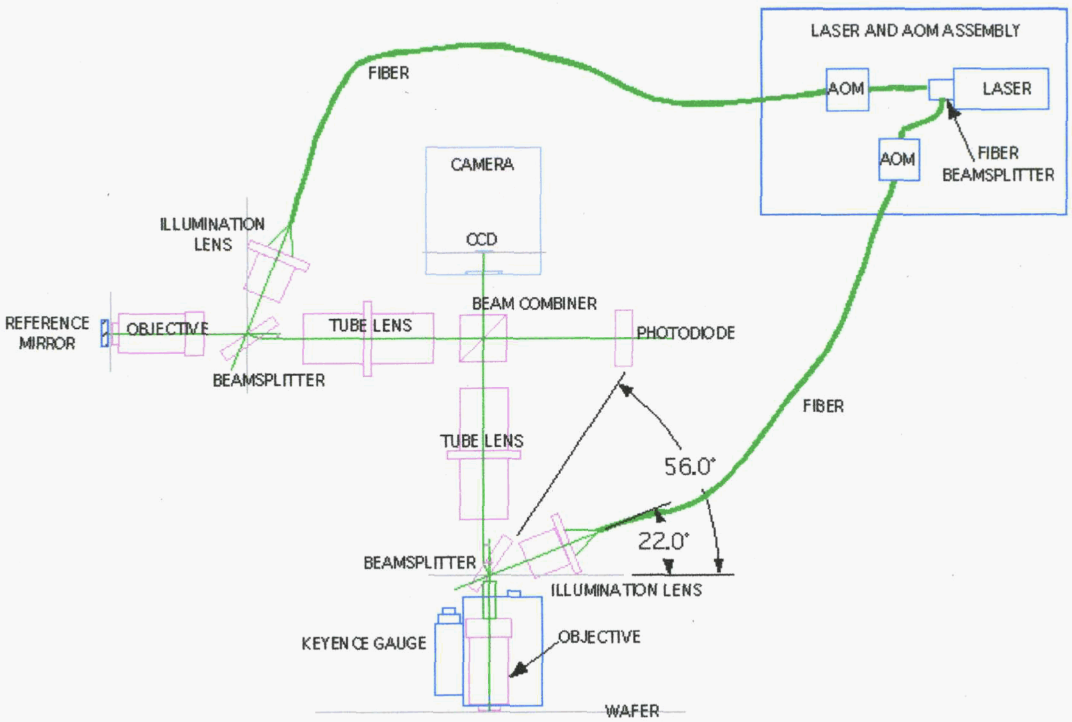

Figure 3. Optical system layout

VAT System Control

This subtask was responsible for control of the various components (Laser, Acousto Optic Modulators (AOMs), Stages, Camera, and Power meter). Figure 4 shows an overall view of the VAT system control. In this task, control computers were specified and acquired, hardware for communication with subsystems was specified and acquire, and software was written to enable long term scanning of semiconductor wafers through a graphical user interface. In order to make this a tool for experimentation and learning, the software system needed to allow for flexibility to change any components setup values. Figure 5 shows the user interface developed under this task. This interface allows the user to select each component of the VAT system for setup. Once the component is selected, a setup screen for that particular component is presented with options for the various available parameters. In this fashion, the software is able to restrict the values for some options for reasons of safety and protection of the equipment.

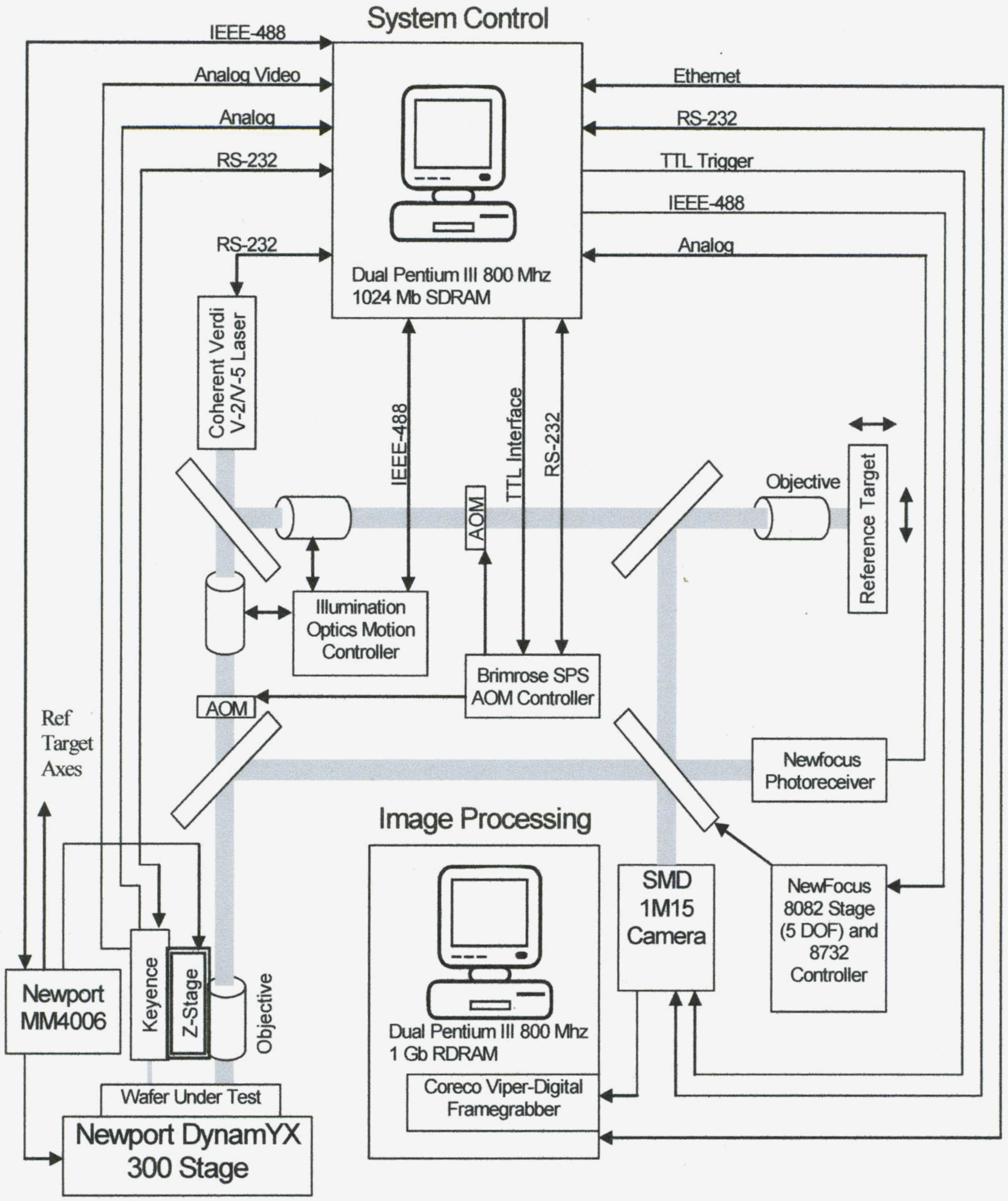

Figure 4. VAT control system layout.

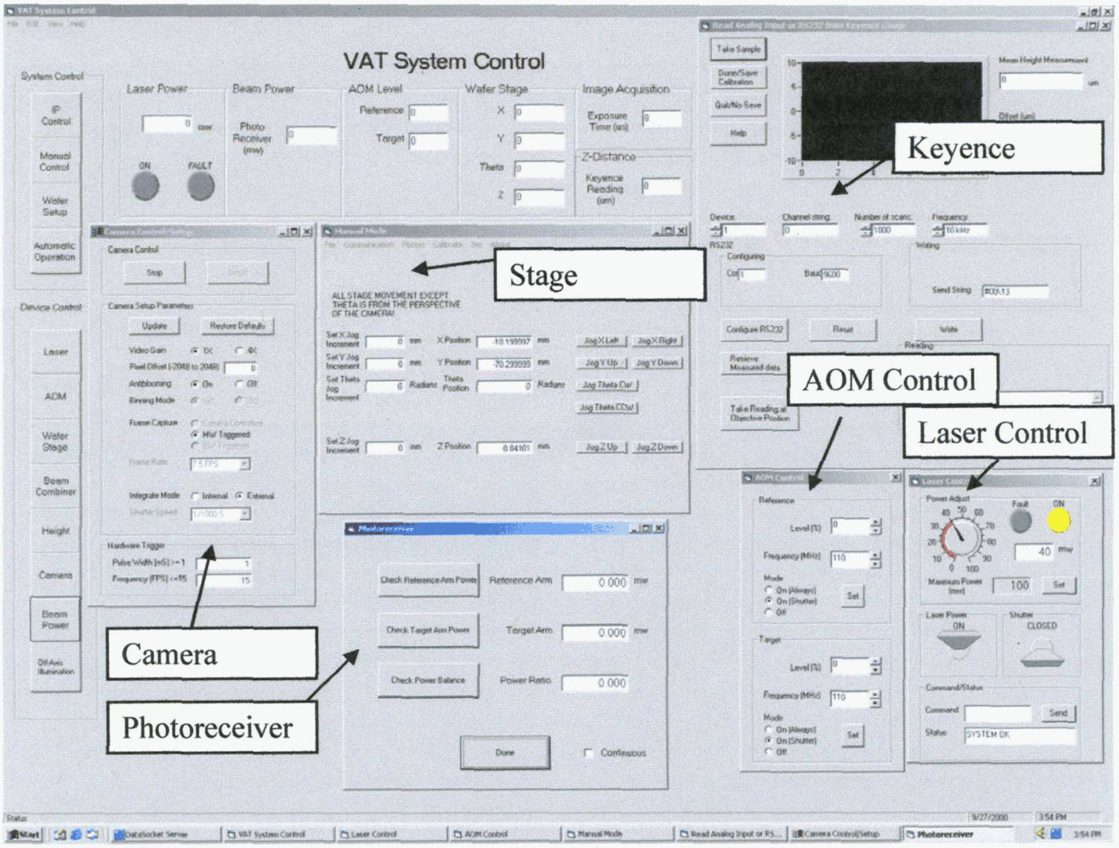

Figure 5. VAT control system interface.

VAT Image Processing

Image processing for the DDH wafer inspection tools required software and algorithm development for image reconstruction and defect detection. In this subtask software was developed to allow the user to select various reconstruction parameters and obtain the resulting phase and magnitude images from the reconstruction. For defect detection, software and algorithms were developed to aligned images from a previous die on the semiconductor wafer to the current die on the wafer, subtract the aligned images, filter to remove edge noise, and locate defects within the image. Further processing was performed when comparing to a third die to determine which die contains the located defects. Figure 6 shows and example of the image processing interface. The flow from reconstruction to defect detection is depicted on the left side of the screen. When a user selects any of the major steps in the image processing chain, available parameters for that step are displayed on the left for modification.

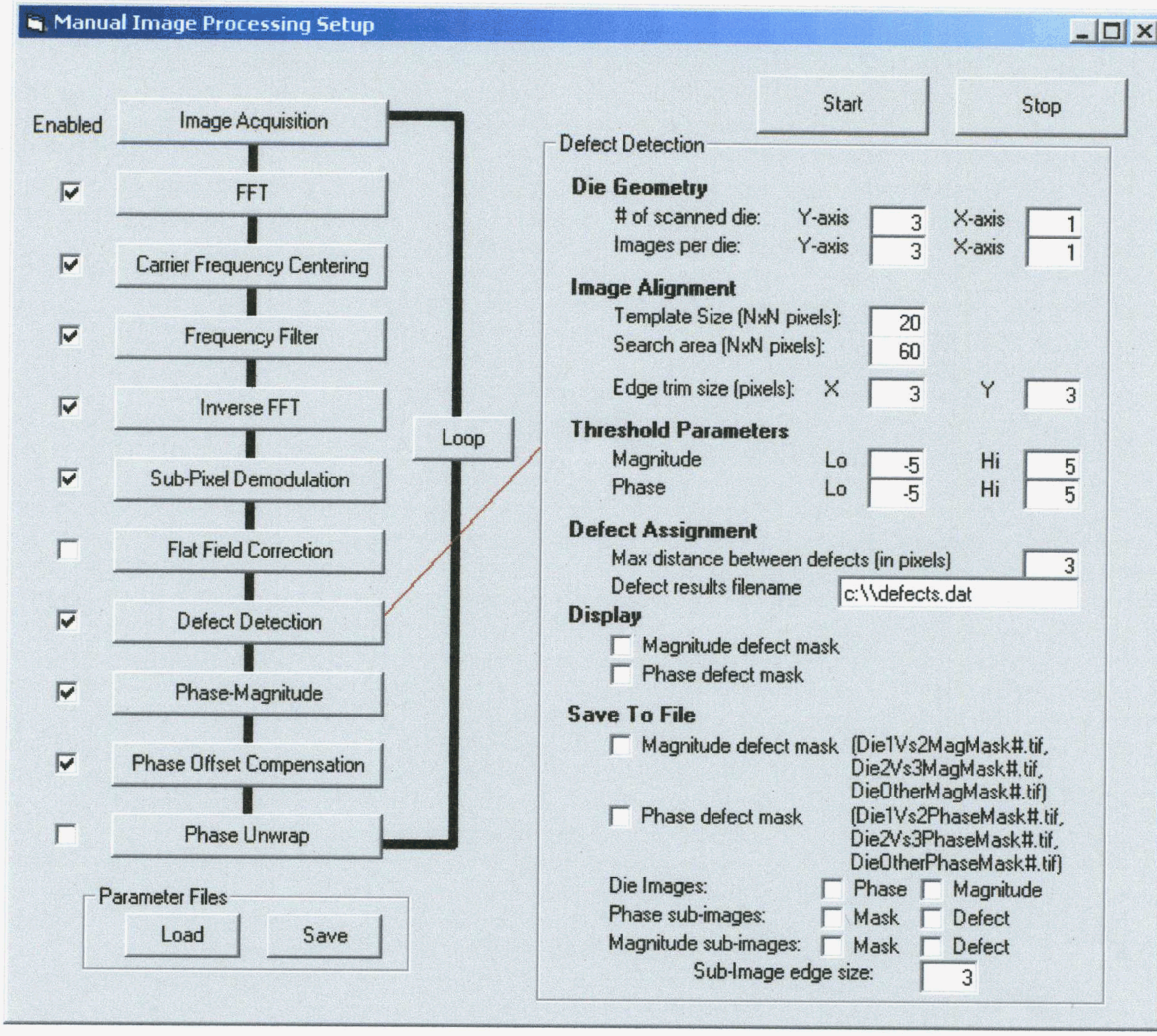

Figure 6. VAT image processing interface.

VAT Results

The key area of interest for DDH in semiconductor inspection is the location of defects in high aspect ratio (HAR) structures. As an example of a result from the VAT, figure 7 shows the phase image of an array of HAR vias in a test wafer provided by International Sematech. The vias on this wafer are 220nm in diameter and are on a 660nm pitch. The vias have an aspect ratio of 6.8 to 1, so they are 1500nm deep. One via in the array has extra material in the bottom making it only 1400nm deep. In the phase image, this defect via is very obvious showing the capability of DDH for location of defects in HAR structures.

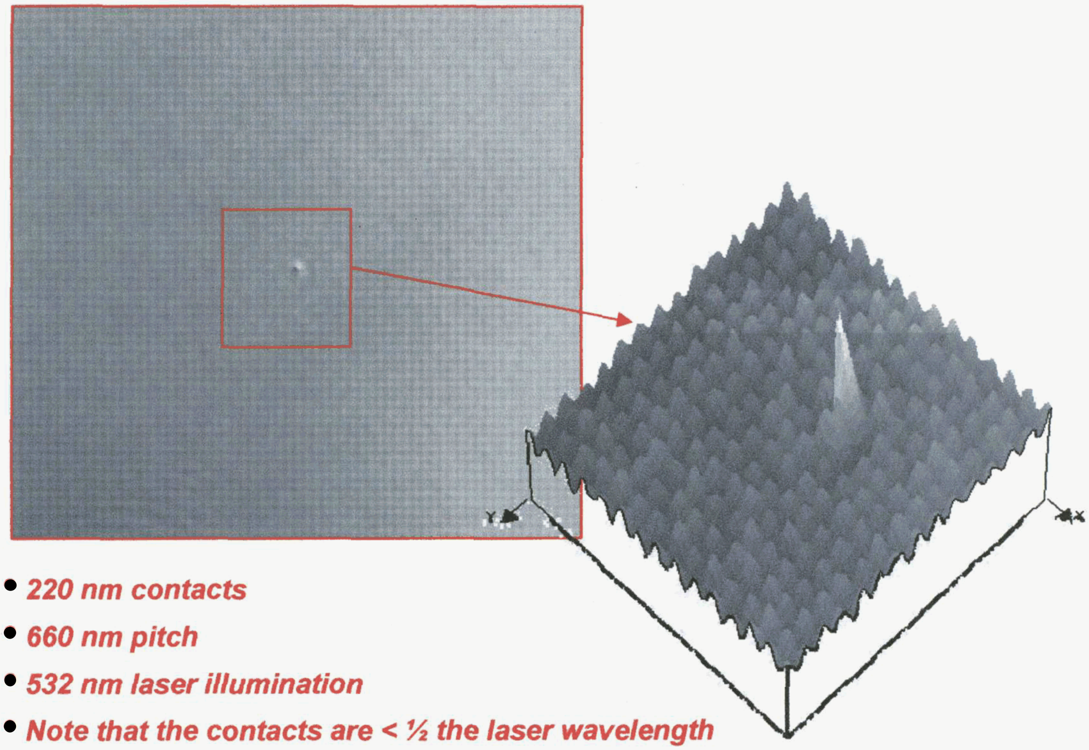

Figure 7. VAT defect detection example.

Processing system design for next generation tool

While the VAT was built for flexibility and low speed, the first generation tools for commercial testing must run at much higher rates of speed. This requires a high power compute engine to reconstruct images and perform defect detection. In this task a study was performed to evaluate and identify an optimum method for accomplishing 2-D high-resolution image analysis for frame-to-frame comparisons in real-time DDH. The intent was to develop an approach that offers flexibility and affordability in a product for the commercial sector. The purpose of the study is to recommend the hardware and software that will be used to develop a system capable of the data acquisition, processing, and control requirements of EAT and BETA I.

The systems require a frame processing throughput capacity of 15 2K-by-2K frames per second initially with an expandable architecture capable of riskless growth to a rate of 30 2K-by-2K frames per second. In addition to achieving the necessary processing throughput, the chosen architecture had to be capable of image acquisition and any real-time control required by the overall system.

Within this task a set of computing and hardware interface requirements were developed and distributed to a number of parallel processing hardware/software vendors along with a request for proposed solutions. This process resulted in ~7 proposed architectures.

Upon review of these proposals, the candidate architectures were narrowed to a couple. At this point nLine made visits to the vendors to determine their capabilities for supplying the systems. Finally, a system was selected by a joint nLine/ORNL committee. This hardware architecture was later implemented in the DAT and EAT systems.

Image Processing Support

While the ORNL staff provided support and assistance on many image processing issues, one area where ORNL took the lead was in off-axis fusion. In this task, algorithms and software were developed to fuse off-axis images to obtain a higher resolution image than is possible with a single on-axis image. An example of the results is shown in Figure 8. The ideal amplitude and phase image are shown on the left. In any optical system, the resolution is limited by the transfer function of the optical system. The center pair of images show the amplitude and phase images that would be captured by the VAT with a single on axis image. Due to the reconstruction in the Fourier domain and the ability to drive the illumination beam off axis, the VAT is able to reconstruct images taken at a continuum of angles. Each of these off axis images provide more information in the frequency domain. By fusing these images, a higher resolution image can be obtained. The last pair of images show results from the fusion algorithm developed under this task and show a marked improvement in resolution over the on-axis image.

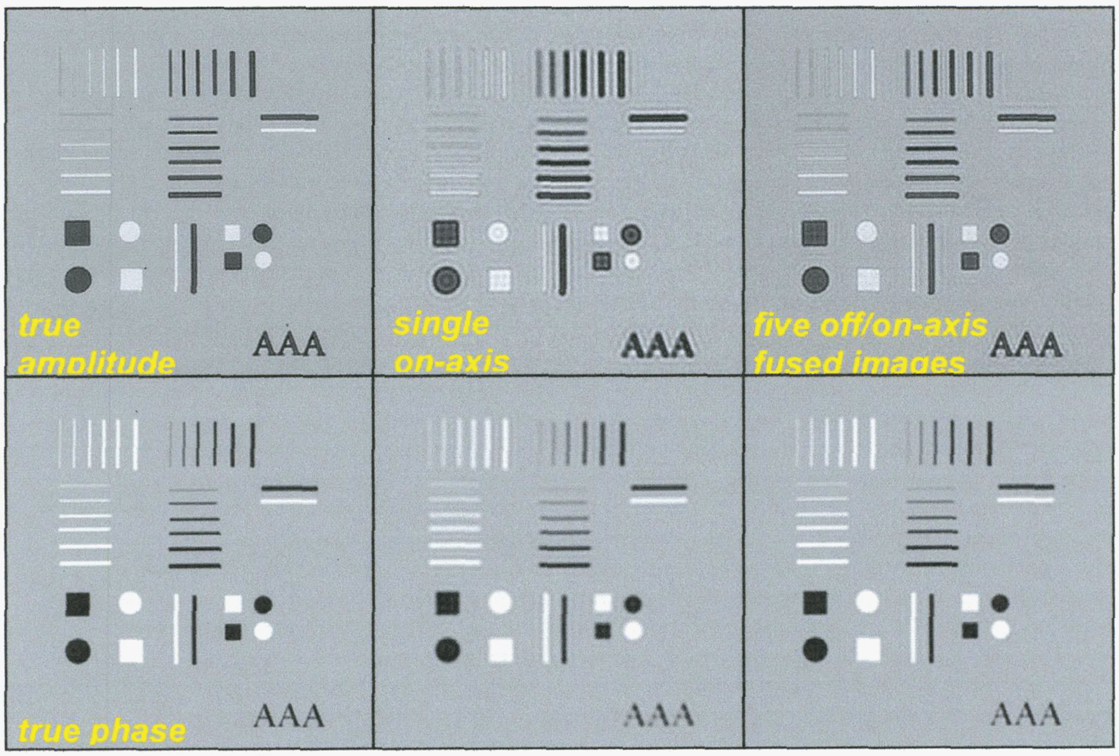

Figure 8. Off-axis fusion example.

Subject Inventions (As defined in the CRADA)

The off axis fusion algorithm developed under this CRADA was submitted as an invention disclosure and is now a patent. Patent 6747771 – "Off-axis illumination direct-to-digital holography ".

Commercialization Possibilities

nLine corporation is still working on commercialization of the DDH technique for industrial inspection. Due to financial issues and changes in the semiconductor market, they are currently in the process of being acquired by another company. ORNL's Technology Transfer and Economic Development (TTED) Organization is in regular and ongoing communications with nLine regarding licenses and intellectual property.

Plans for Future Collaboration

ORNL is still connected to nLine through licensing agreements and we hope to work with the eventual owners in further development of the technology. During this and other work on DDH we have developed ideas for application of this technology to other areas such as MEMS inspection and lithography mask inspection and hope to pursue these as well.

Conclusions

This CRADA was very successful in obtaining goals outlined in the original SOW. With this CRADA, we were able to prove DDH's capability in semiconductor wafer inspection. Unfortunately, nLine has experience some financial difficulties that has slowed the further introduction of this technology into the market. The VAT tool developed at ORNL has remained very stable and has outperformed original expectations. Through the inclusion of off-axis fusion, this tools resolution can be further extended and will hopefully find other applications.